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Phase Locked Loop using Standard Cell in 45nm CMOS Technology

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***Abstract*—Phase Locked Loop (PLL) is a control system used for synchronization to achieve same frequency. It is used in clock generation, clock recovery. In this paper, a 1.1 V, operating at 400MHz phase-locked loop implemented in 45 nm CMOS technology using standard cell i.e phase frequency detector uses D Flip-Flop and NAND gate using standard cell .The output from the PFD is connected to the low pass filter which is designed using capacitor and resistor in which the overall area of the circuit is reduced. The loop filter is passive for less area. Phase lock loop produces an output frequency match with the frequency of an input signal. The designed PLL has the operating frequency of 1.6 GHz. The voltage controlled oscillator used is current starved voltage controlled .For low power the PFD uses D Flip-Flop which produces low power Phase Locked Loop. The voltage controlled oscillator produces output frequency and high gain. Some of the performance parameters to be considered are locking range , tracking range .Higher bandwidth is provided to prevent noise and passive loop filter for stability .Since today's communication media uses phase locked loop in GHz range .The work focuses on reconstruction of PLL in GHz range using standard cell layout design.**

***Index Terms*— CMOS Technology, current starved VCO, Phase Frequency Detector, Charge Pump, Low Pass Filter.**

I. INTRODUCTION

In 1930's for the first time the concept of Phase Locked Loops (PLL) came into existence. But for now, the cost required to develop this PLL is high. Due to the development in the integrated circuits, PLL has become one of the major control systems in the electronics today. The concept of phase-locked loop (PLL) was found and its functions were described and used since 1922. The methods involved in these applications are more complicated. Most of the PLL operates at GHz frequency range. In other communication system say FM and AM demodulation the PLL's operates at low frequencies say 100MHz, monolithic PLLs are in use because of their low cost and high performance. Phase locked loops produces an output frequency match with the frequency of an input signal. Any change in frequency and the phase results in locking. This phase and frequency change is said to be an error .VCO is used to tune the input frequency and produces oscillation frequency. The locking of phase and frequency between input and the oscillator is termed as phase-locked loop (PLL).

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II. LITERATURE SURVEY

The author Neil H.E. Weste, et al. explained about how low noise PLLs are designed i.e. loop filter should have high bandwidth to remove the noise[1. In 19th century, Rayleigh explained about the how weakly coupled tuning forks were synchronized to oscillate at same frequency [2].The author W.H Eccles and J. H. Vincent how the two electronic oscillators which oscillated at different frequencies were made to oscillate at the same frequency[3]. Edwin Armstrong explained that in super-heterodyne receiver the local oscillator was tuned to the required frequency and it is being multiplied with the input signal and later it was named as Phase Locked Loop. Since the local oscillator would change its frequency all the times it required a control signal was applied to the oscillator, to maintain the phase and frequency of the input signal same as output signal. This method was described by Henri de-Bellescize in 1932 [4].The author Edward Victor Appleton explained about synchronization of oscillators in 1923[5]. After this there was a lot of researches done in 1940s the first and foremost interest was given for a local oscillator in FM demodulation. The phase-locked loops was developed had feedback amplifiers. The methods of maintaining the stability of feedback are determined. Signets explained about monolithic IC's like the NE565 which were of low frequency and low cost [6].

III. PROPOSED METHODOLOGY

Standard cell design is the design of application-specific integrated circuits (ASICs) using digital-logic The standard cell has many transistor structures such as basic gates that provides a Boolean variables and some sequential circuits like D Flip-Flop and Latches. Even though these structures are highly complex. The structure's functional behavior is determined using truth table and Boolean equation. Here PLL is designed using standard cell. PFD has D Flip-Flop and Nand gate which are designed using standard cell.

A Phase Locked Loops (PLL) has a negative feedback control system whose input frequency is similar to output frequency. One of the input signal given from reference clock and the other signal is given as feedback to the phase frequency detector from the voltage controlled oscillator. The error signal which is produced by the phase frequency detector is fed into loop filter which removes high frequency components and allow only low frequency components. The output of the loop filter is given to the voltage controlled oscillator which maintains the reference frequency and the feedback frequency to be in-phase. Any change in frequency and the phase results in locking. This phase and frequency change is said to be an error. Initially loop will be out of lock, later by changing the reference frequency by keeping the voltage controlled oscillator frequency constant ,lock condition can be achieved. The functional block diagram of PLL consists of three parts they are shown in below figure1

- Phase Frequency Detector (PFD)
- Loop filter (LF)
- Voltage controlled oscillator (VCO)

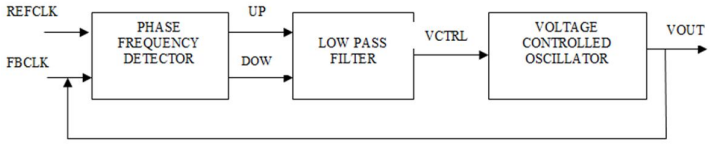

Figure1. Functional block diagram of Phase locked loop

A. Phase Frequency detector

Phase frequency detector is also called as phase comparator which compares the phase of two input signal. One from the reference clock and other from the voltage controlled oscillator which is fed back to phase frequency detector. The phase detector used in PLL here is digital. Phase Frequency Detector (PFD) consists of two D-type flip flops with NAND gate in series. Here the D Flip-Flop used has asynchronous reset circuitry .The phase frequency detector produces two outputs namely UP and DOWN signal. When reference signal leads the feedback signal UP signal will be produced. When reference signal lags the feedback signal DOWN signal will be produced as shown in the below figure3. The two signals then enter the loop filter whose stability and the phase error are checked. Since the signals are of low frequency, it would not be removed by the loop filter and would results in spurs in the VCO called "dead zone" effect.

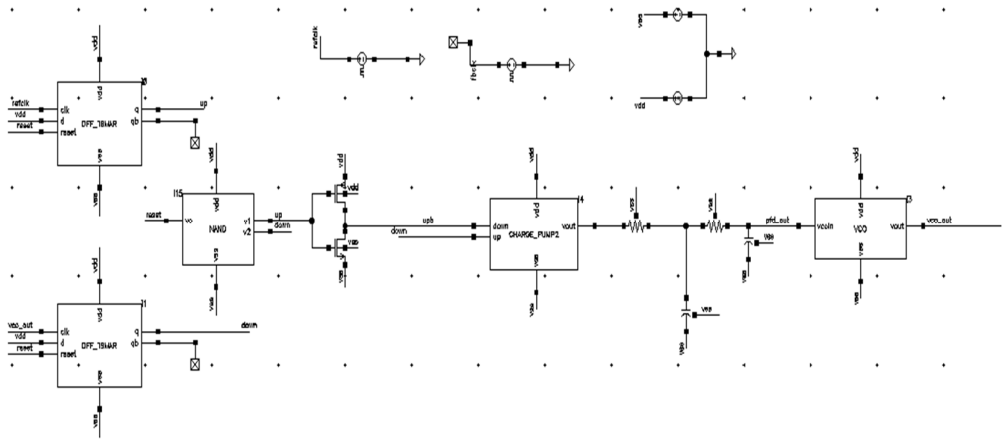

Figure2. Schematic of Phase locked loop

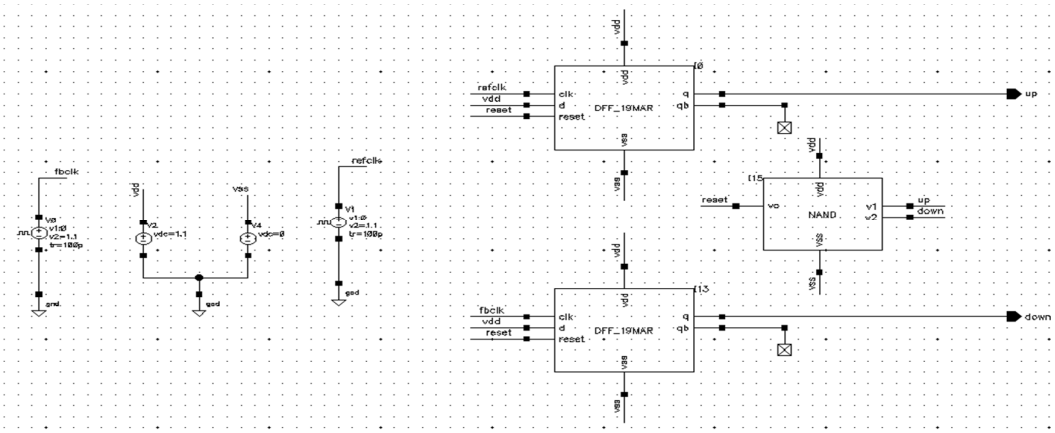

Figure3. Phase frequency detector

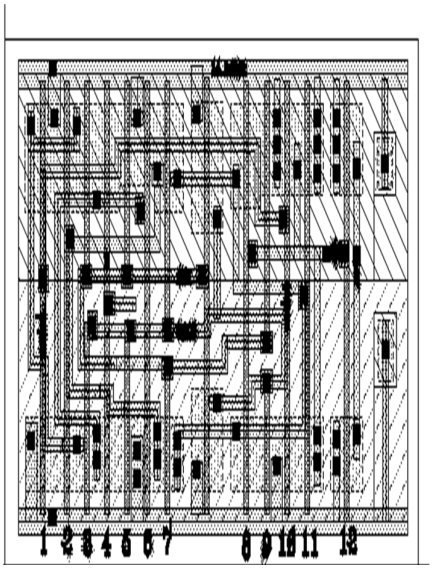

Figure4.Standard cell layout of D Flip-Flop

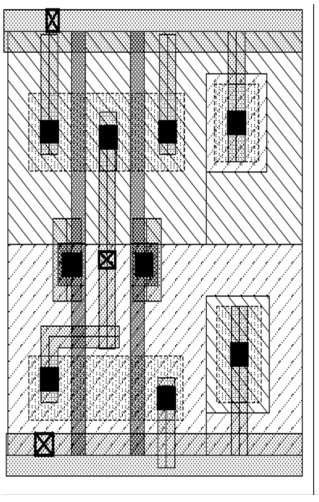

Figure5.Standard cell layout of NAND gate

B. Loop filter

The loop filter used is passive filter because which requires less area. The output of phase frequency detector i.e UP and DOWN signals are given to loop filter which removes high frequency and maintains stability. The difference between the frequency of two input signals i.e reference signal and the feedback signal which is called as error voltage is reduced . Since the PLL is a negative feedback system there is a necessity to maintain the stable system. Hence loop filters are recommended. In order to remove noise loop filters are provided higher bandwidth. Some of the performance parameter which can be measured here are capture range, lock range and bandwidth. The capture range is the range in which the Phase Locked Loop attains the Phase Lock. The tracking range is the range of frequency where the output VCO frequency is kept constant and input frequency is varied.

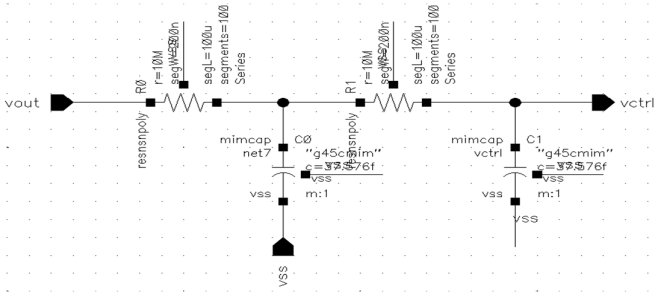

Figure6. Low pass filter

C. Voltage controlled oscillator (VCO)

The aim of the VCO is to produce oscillation frequency which operates in GHz range. The VCO provides square wave, triangular wave and sine wave outputs depending on the types of oscillators used. The output frequency is determined by Vctrl applied to the control terminal of VCO. By varying the voltage control the frequency is adjusted such that the input frequency varies and the VCO frequency is kept constant which is called tracking. Here the input reference frequency and the output oscillation frequency are same.

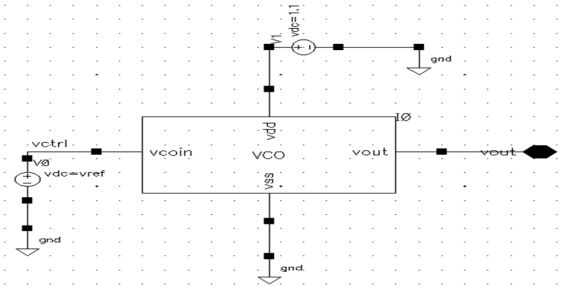

Figure7. Voltage controlled oscillator

When control voltage of 0.583v is given the central frequency is 1.6 GHz is obtained. For different control voltage's different oscillation frequency ranging from 8.11 MHz to 3.44 GHz is obtained shown in table I.

IV. CONCLUSION AND RESULT

The phase locked loop is the control system which is used in communications in clock synthesis, clock recovery, frequency synthesizers. In present day communication phase locked loop operates in GHz frequency range .In this project 1.1 V, operating at 400MHz PLL is implemented on CADENCE gpdk45nm process technology with an improved lock range 386MHz. Proposed PFD has dead zone and it has less area as compared to conventional PFD due to presence of reset circuitry, also high gain 4.29GHz/V, larger tuning range 8.11MHz – 3.44GHz, Damping factor is 1.5 and the center frequency is 1.6MHz is achieved in designed CS-VCO. Simulation of this PLL circuit is done using spectre simulator of CADENCE and improved simulation results are obtained. Below table shows the comparative analysis of phase locked loop with the reference paper is show below in table II.

TABLE I: TUNING RANGE OF VCO

Control voltage (v)	Oscillation frequency (Hz)
0.35	8.11M
0.4	23.3M
0.45	58.58M
0.5	130.89M
0.55	259.0M
0.6	491.1M
0.65	819.6M
0.7	1.21M
0.75	1.64M
0.8	2.06G
0.85	2.336G
0.9	2.76G
0.95	3.01G
1.0	3.18G
1.1	3.44G

TABLE II: COMPARATIVE ANALYSIS

Parameter	**Specification (this work)**	**Specification (Reference)**
Technology	45nm	45nm
Reference frequency	400MHz	-
Operating voltage	1.1v	1.1v
Center frequency	1.6GHz	1GHz
Oscillation frequency	386GHz	-
Locking range	0.583v	-
Tuning range	8.11MHz to 3.44GHz	8MHz to 7.4GHz
Gain	4.29GHz	3.93
Damping factor	1.5	-

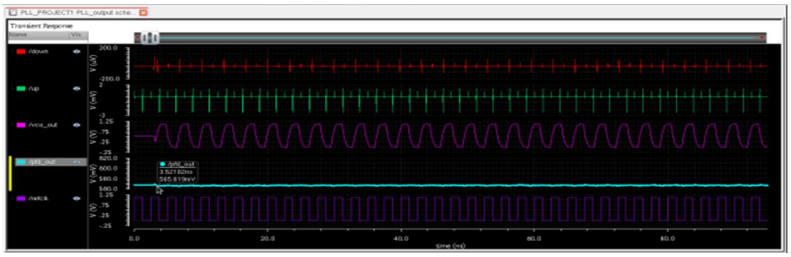

Figure 8. Simulation of Phase locked loop

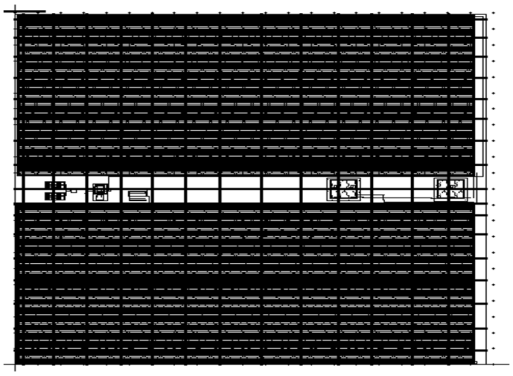

Figure 9. Layout of Phase locked loop

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